I claim:

1. A program-controlled unit, comprising:

an intelligent core configured to process instructions to be executed;

a plurality of units selected from the group consisting of internal peripheral units disposed inside the program-controlled unit, external peripheral units exterior to the program-controlled unit, and one or more memory devices;

a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting said intelligent core and said units, including an interface connection between said intelligent core and said internal peripheral units, between said intelligent core and said external peripheral units, between said intelligent core and said memory devices, and between said plurality of units; and

wherein said structurable hardware unit is configured to evaluate and process data and/or signals received thereby.

2. The program-controlled unit according to claim 1, wherein said structurable hardware unit is disposed in circuit terms between said intelligent core and said plurality of units.

3. The program-controlled unit according to claim 1, wherein said structurable hardware unit is connected to a multiplicity of potential data and signal sources and data and signal destinations, and wherein a plurality of multiplexers are connected to said structurable hardware unit for selecting current data and signal sources and current data and signal destinations.

4. The program-controlled unit according to claim 3, wherein the data and signal sources and the data and signal destinations comprise units selected from the group of units consisting of said intelligent core, said peripheral units, said memory devices, and portions of said structurable hardware unit.

5. The program-controlled unit according to claim 1, wherein a structuring of said structurable hardware unit selectively results in an alteration of given data paths and in a configuration of logic elements.

6. The program-controlled unit according to claim 1, wherein said structurable hardware unit comprises a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal, said logic block unit enabling devices to be connected via said structurable hardware unit to cooperate as desired.

7. The program-controlled unit according to claim 6, wherein said clock generation unit and said logic block unit each contain configurable elements.

8. The program-controlled unit according to claim 6, wherein said clock generation unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

9. The program-controlled unit according to claim 6, wherein the logic block unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

10. The program-controlled unit according to claim 6, wherein said logic block unit comprises at least one logic block subdivided at least partly into individually configurable sub-blocks with predetermined tasks.

11. The program-controlled unit according to claim 10, wherein one of said sub-blocks is configured as a processing device enabled for one of arithmetic and logical processing of data input to said sub-block.

12. The program-controlled unit according to claim 10, wherein one of said sub-blocks is configured as a state machine for central sequence control.

13. The program-controlled unit according to claim 10, wherein one of said sub-blocks is configured as an address calculation device for calculating source and destination addresses.

14. The program-controlled unit according to claim 10, wherein one of said sub-blocks is configured as an instruction injection device for injecting instructions into an instruction pipeline of said intelligent core.

15. The program-controlled unit according to claim 1, wherein said structurable hardware unit is configurable with devices selected from the group consisting of fuses and anti-fuses.

16. The program-controlled unit according to claim 1, wherein said structurable hardware unit is reversibly configurable.

17. The program-controlled unit according to claim 16, wherein said structurable hardware unit is configurable based on data representing a desired configuration, and the data are

stored in memory devices insertible into a memory or I/O area which is addressible by said intelligent core.

18. The program-controlled unit according to claim 1, wherein a configuration of said structurable hardware unit is enabled only at predetermined times.

19. The program-controlled unit according to claim 1, wherein a configuration of said structurable hardware unit is enabled at any time.

20. A program-controlled unit, comprising:

an intelligent core having an instruction pipeline and processing instructions to be executed;

a plurality of units selected from the group consisting of internal peripheral units disposed inside the program-controlled unit, external peripheral units exterior to the program-controlled unit, and one or more memory devices;

a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting said intelligent core and said units, including an interface connection between said intelligent core and said internal peripheral units, between said intelligent core and said external peripheral units,

between said intelligent core and said memory devices, and between said plurality of units; and

wherein said structurable hardware unit is configured to inject instructions into said instruction pipeline of said intelligent core.

21. The program-controlled unit according to claim 20, wherein said structurable hardware unit is disposed in circuit terms between said intelligent core and said plurality of units.

22. The program-controlled unit according to claim 20, wherein said structurable hardware unit is connected to a multiplicity of potential data and signal sources and data and signal destinations, and wherein a plurality of multiplexers are connected to said structurable hardware unit for selecting current data and signal sources and current data and signal destinations.

23. The program-controlled unit according to claim 22, wherein the data and signal sources and the data and signal destinations comprise units selected from the group of units consisting of said intelligent core, said peripheral units, said memory devices, and portions of said structurable hardware unit.

24. The program-controlled unit according to claim 20, wherein a structuring of said structurable hardware unit selectively results in an alteration of given data paths and in a configuration of logic elements.

25. The program-controlled unit according to claim 20, wherein said structurable hardware unit comprises a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal, said logic block unit enabling devices to be connected via said structurable hardware unit to cooperate as desired.

26. The program-controlled unit according to claim 25, wherein said clock generation unit and said logic block unit each contain configurable elements.

27. The program-controlled unit according to claim 25, wherein said clock generation unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

28. The program-controlled unit according to claim 25, wherein the logic block unit is formed at least in part by a device selected from the group consisting of a DNF logic

configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

29. The program-controlled unit according to claim 25, wherein said logic block unit comprises at least one logic block subdivided at least partly into individually configurable sub-blocks with predetermined tasks.

30. The program-controlled unit according to claim 29, wherein one of said sub-blocks is configured as a processing device enabled for one of arithmetic and logical processing of data input to said sub-block.

31. The program-controlled unit according to claim 29, wherein one of said sub-blocks is configured as a state machine for central sequence control.

32. The program-controlled unit according to claim 29, wherein one of said sub-blocks is configured as an address calculation device for calculating source and destination addresses.

33. The program-controlled unit according to claim 29, wherein one of said sub-blocks is configured as an instruction injection device for injecting instructions into said instruction pipeline of said intelligent core.

34. The program-controlled unit according to claim 20, wherein said structurable hardware unit is configurable with devices selected from the group consisting of fuses and anti-fuses.

35. The program-controlled unit according to claim 20, wherein said structurable hardware unit is reversibly configurable.

36. The program-controlled unit according to claim 35, wherein said structurable hardware unit is configurable based on data representing a desired configuration, and the data are stored in memory devices insertible into a memory or I/O area which is addressible by said intelligent core.

37. The program-controlled unit according to claim 20, wherein a configuration of said structurable hardware unit is enabled only at predetermined times.

38. The program-controlled unit according to claim 20, wherein a configuration of said structurable hardware unit is enabled at any time.

39. A program-controlled unit, comprising:

an intelligent core configured to process instructions to be executed;

a plurality of units selected from the group consisting of internal peripheral units disposed inside the program-controlled unit, external peripheral units exterior to the program-controlled unit, and one or more memory devices;

a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting said intelligent core and said units, including an interface connection between said intelligent core and said internal peripheral units, between said intelligent core and said external peripheral units, between said intelligent core and said memory devices, and between said plurality of units; and

wherein said structurable hardware unit is configured to generate and to output signals selected from the group consisting of interrupt requests and event-signaling messages.

40. The program-controlled unit according to claim 39, wherein said structurable hardware unit is disposed in circuit terms between said intelligent core and said plurality of units.

41. The program-controlled unit according to claim 39, wherein said structurable hardware unit is connected to a multiplicity of potential data and signal sources and data and signal destinations, and wherein a plurality of multiplexers are connected to said structurable hardware unit for selecting current data and signal sources and current data and signal destinations.

42. The program-controlled unit according to claim 41, wherein the data and signal sources and the data and signal destinations comprise units selected from the group of units consisting of said intelligent core, said peripheral units, said memory devices, and portions of said structurable hardware unit.

43. The program-controlled unit according to claim 39, wherein a structuring of said structurable hardware unit selectively results in an alteration of given data paths and in a configuration of logic elements.

44. The program-controlled unit according to claim 39, wherein said structurable hardware unit comprises a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal, said logic block unit enabling devices to be connected via said structurable hardware unit to cooperate as desired.

45. The program-controlled unit according to claim 44, wherein said clock generation unit and said logic block unit each contain configurable elements.

46. The program-controlled unit according to claim 44, wherein said clock generation unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

47. The program-controlled unit according to claim 44, wherein the logic block unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

48. The program-controlled unit according to claim 44, wherein said logic block unit comprises at least one logic block subdivided at least partly into individually configurable sub-blocks with predetermined tasks.

49. The program-controlled unit according to claim 48, wherein one of said sub-blocks is configured as a processing device enabled for one of arithmetic and logical processing of data input to said sub-block.

50. The program-controlled unit according to claim 48, wherein one of said sub-blocks is configured as a state machine for central sequence control.

51. The program-controlled unit according to claim 48, wherein one of said sub-blocks is configured as an address calculation device for calculating source and destination addresses.

52. The program-controlled unit according to claim 48, wherein one of said sub-blocks is configured as an instruction injection device for injecting instructions into an instruction pipeline of said intelligent core.

53. The program-controlled unit according to claim 39, wherein said structurable hardware unit is configurable with devices selected from the group consisting of fuses and anti-fuses.

54. The program-controlled unit according to claim 39, wherein said structurable hardware unit is reversibly configurable.

55. The program-controlled unit according to claim 54, wherein said structurable hardware unit is configurable based

on data representing a desired configuration, and the data are stored in memory devices insertible into a memory or I/O area which is addressible by said intelligent core.

56. The program-controlled unit according to claim 39, wherein a configuration of said structurable hardware unit is enabled only at predetermined times.

57. The program-controlled unit according to claim 39, wherein a configuration of said structurable hardware unit is enabled at any time.

58. A program-controlled unit, comprising:

an intelligent core configured to process instructions to be executed;

a plurality of units selected from the group consisting of internal peripheral units disposed inside the program-controlled unit, external peripheral units exterior to the program-controlled unit, and one or more memory devices;

a structurable hardware unit selectively forming an application-specifically configurable intelligent interface for respectively connecting said intelligent core and said units, including an interface connection between said intelligent core and said internal peripheral units, between

said intelligent core and said external peripheral units, between said intelligent core and said memory devices, and between said plurality of units; and

wherein said structurable hardware unit is configured to selectively react to interrupt requests or other event-signaling messages from devices connected thereto and prevent the interrupt requests or the event-signaling messages from being forwarded.

59. The program-controlled unit according to claim 58, wherein said structurable hardware unit is disposed in circuit terms between said intelligent core and said plurality of units.

60. The program-controlled unit according to claim 58, wherein said structurable hardware unit is connected to a multiplicity of potential data and signal sources and data and signal destinations, and wherein a plurality of multiplexers are connected to said structurable hardware unit for selecting current data and signal sources and current data and signal destinations.

61. The program-controlled unit according to claim 60, wherein the data and signal sources and the data and signal destinations comprise units selected from the group of units

consisting of said intelligent core, said peripheral units, said memory devices, and portions of said structurable hardware unit.

62. The program-controlled unit according to claim 58, wherein a structuring of said structurable hardware unit selectively results in an alteration of given data paths and in a configuration of logic elements.

63. The program-controlled unit according to claim 58, wherein said structurable hardware unit comprises a clock generation unit generating a clock signal and a logic block unit connected to receive the clock signal, said logic block unit enabling devices to be connected via said structurable hardware unit to cooperate as desired.

64. The program-controlled unit according to claim 63, wherein said clock generation unit and said logic block unit each contain configurable elements.

65. The program-controlled unit according to claim 63, wherein said clock generation unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

66. The program-controlled unit according to claim 63, wherein the logic block unit is formed at least in part by a device selected from the group consisting of a DNF logic configuration, a NAND array, a multiplexer-based logic variant, and a structurable logic configuration.

67. The program-controlled unit according to claim 63, wherein said logic block unit comprises at least one logic block subdivided at least partly into individually configurable sub-blocks with predetermined tasks.

68. The program-controlled unit according to claim 67, wherein one of said sub-blocks is configured as a processing device enabled for one of arithmetic and logical processing of data input to said sub-block.

69. The program-controlled unit according to claim 67, wherein one of said sub-blocks is configured as a state machine for central sequence control.

70. The program-controlled unit according to claim 67, wherein one of said sub-blocks is configured as an address calculation device for calculating source and destination addresses.

71. The program-controlled unit according to claim 67, wherein one of said sub-blocks is configured as an instruction injection device for injecting instructions into an instruction pipeline of said intelligent core.

72. The program-controlled unit according to claim 58, wherein said structurable hardware unit is configurable with devices selected from the group consisting of fuses and anti-fuses.

73. The program-controlled unit according to claim 58, wherein said structurable hardware unit is reversibly configurable.

74. The program-controlled unit according to claim 73, wherein said structurable hardware unit is configurable based on data representing a desired configuration, and the data are stored in memory devices insertible into a memory or I/O area which is addressible by said intelligent core.

75. The program-controlled unit according to claim 58, wherein a configuration of said structurable hardware unit is enabled only at predetermined times.

76. The program-controlled unit according to claim 58, wherein a configuration of said structurable hardware unit is enabled at any time.